REMARKS

At the outset, the Examiner is thanked for the thorough consideration given the subject application. Claims 1-12 are currently pending, claims 1, 5, 7, and 9 have been amended, and claims 11 and 12 have been withdrawn from consideration as being drawn to a non-elected invention. Minor changes have been made to the specification to correct informalities. No new matter has been added. Reconsideration and reexamination are respectfully requested.

The Examiner rejected claims 1-10 under 35 USC 103(a) as being unpatentable over AF1-2 (Applicants' Figures 1-2) in view of Nishikawa et al. (US Patent No. 5,724,107). Applicants respectfully traverse this rejection.

Claim 1 is allowable at least for the reason that claim 1 recites a combination of elements including a capacitor lower electrode of a storage capacitor formed on the same plane as a gate line; a capacitor upper electrode formed integrally with the drain electrode on the capacitor lower electrode; a first insulation film inserted between the capacitor upper electrode and the capacitor lower electrode; and a thin film transistor array substrate connected with the drain electrode and including a reflective electrode formed at the pixel areas and formed above and connected to the drain electrode.

Claim 5 is allowable at least for the reason that claim 5 recites a combination of elements including a capacitor lower electrode of a storage capacitor formed on the same plane as a gate line; a capacitor upper electrode formed integrally with the drain electrode on the capacitor lower electrode; a first insulation film inserted between the capacitor upper electrode and the capacitor lower electrode; a reflective electrode connected with the drain electrode and formed on the reflection area above the drain electrode.

None of the cited references, singly or in combination, teaches or suggests at least these features of the invention.

On page 3 of the Office Action, the Examiner alleges that AF1-2 do not disclose a capacitor upper electrode formed integrally with the drain electrode on the capacitor lower electrode. The Examiner cites Nishikawa et al. in an attempt to cure the deficiencies of AF1-2.

In AF1-2, the capacitor upper electrode is formed separately from the drain electrode. In Nishikawa et al., the source electrode is connected with the pixel electrode and the capacitor upper electrode is the pixel electrode. In contrast, in the present invention, the capacitor upper electrode is formed integrally with the drain electrode and the reflective electrode is formed above and connected to the drain electrode as in claims 1 and 5. Nishikawa et al. fails to cure the deficiencies of AF1-2.

Applicant respectfully submits that the Examiner has failed to establish a *prima facie* case of obviousness. Applicant respectfully requests that the rejection under 35 USC § 103(a) be withdrawn.

Moreover, claims 2-4 and 6-10 are allowable by virtue of their dependence on claims 1 and 5, which are believed to be allowable.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

If the Examiner deems that a telephone call would further the prosecution of this application, the Examiner is invited to call the undersigned at (202) 496-7371. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the

filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911.

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Respectfully submitted,

By _____

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Version With Markings to Show Changes Made

In the Specification

Please amend the specification as follows:

On page 4, paragraph beginning on line 11;

At this time, on the entire surface of the substrate including the gate line 102, the gate electrode 102a and the capacitor lower electrode 102c is the gate insulation film 103 of silicon[e] nitride (SiN_x) film to insulate upper and lower layers, and an semiconductor layer 104 of an island form between the gate insulation film 103 and the source/drain electrodes 105a and 105b. On the entire surface of the substrate including the data line 105, the source/drain electrodes 105a and 105b and the capacitor upper electrode 105c is a passivation film 106 coated in a prescribed thickness.

On page 6, paragraph beginning on line 9:

In detail, the thin film transistor has a laminated film structure and includes a gate electrode 202a connected to the gate line 202, a gate insulation film 203, which is made of silicon[e] nitride (SiN_x), formed on the entire surface including the gate line 202, an semiconductor layer 204 made of amorphous silicon[e], and source/drain electrodes 205a and 205b connected to the data line 205. A reflective electrode 207a, which will be formed later, is electrically connected with the drain electrode through a pixel contact hole 208 formed by removing the first passivation film on the drain electrode 205b. As a result, a voltage according to the on-off action of the thin film transistor is applied to the reflective electrode 207a.

On page 12, paragraph beginning on line 10:

At this time, the capacitor lower electrode 302c, the gate insulation film 303 and the capacitor upper electrode 305c form a storage capacitor. A laminated structure consisting of the gate electrode 302a, the gate insulation film 303, a semiconductor layer 304 and the source/drain electrodes 305a and 305b forms a thin film transistor. An a-Si:H TFT (amorphous Silicon[e] Thin Film Transistor) having the semiconductor layer 304 made of amorphous silicon[e] is the

main current.

In the Claims

Please amend the claims as follows:

1. (Amended) A reflective liquid crystal display device comprising:

a plurality of gate lines and data lines intersecting on a first substrate, the gate lines and the data lines defining pixel areas;

a plurality of thin film transistors formed at the intersections of the gate lines and the data lines, [the] each thin film transistor including a gate electrode, a semiconductor layer, a source electrode and a drain electrode;

a capacitor lower electrode of a storage capacitor formed on the same plane as [the] a gate line;

a capacitor upper electrode formed integrally with the drain electrode on the capacitor lower electrode;

a first insulation film inserted between the capacitor upper electrode and the capacitor lower electrode; and

a thin film transistor array substrate connected with the drain electrode and including [the] a reflective electrode formed at the pixel areas and formed above and connected to the drain electrode.

5. (Amended) A transflective liquid crystal display device, which has pixel areas defined into a reflection part and a transmission part, the liquid crystal display device comprising:

a plurality of gate lines and data lines intersecting on a first substrate, the gate lines and the data lines defining pixel areas;

a plurality of thin film transistors formed at the intersections of the gate lines and the data lines, [the] each thin film transistor including a gate electrode, a semiconductor layer, a source electrode and a drain electrode;

a capacitor lower electrode of a storage capacitor formed on the same plane as [the] a gate line;

a capacitor upper electrode formed integrally with the drain electrode on the capacitor lower electrode;

a first insulation film inserted between the capacitor upper electrode and the capacitor lower electrode;

a reflective electrode connected with the drain electrode and formed on the reflection area above the drain electrode; and

a thin film transistor array substrate connected with the reflective electrode and including the transmissive electrode formed at the transmission area.

7. (Amended) The transflective liquid crystal display device as claimed in claim 5, wherein the first insulation film is one of silicon[e] nitride (SiNx) and silicon[e] oxide (SiOx).

9. (Amended) The transflective liquid crystal display device as claimed in claim 8, wherein the second insulation film is one of silicon[e] nitride (SiNx), BCB or acryl resin.